# Karim Hassan Senior Hardware Engineer

Holtsville, NY · karim.hassan@gmail.com · +1 631-555-0146 · linkedin.com/in/karimhassan

## PROFILE SUMMARY

- **Senior Hardware Engineer** with **7 years** building rugged devices at **Zebra Technologies** and **Motorola Solutions**, owning the main board of a **rugged Android handheld** from architecture to PVT.
- Works in **Cadence Allegro** and **HyperLynx** on **Arm Cortex-A** boards with **LPDDR5**, USB 3 and MIPI camera links, and automates DVT stations in **Python**.
- Strong in **high-speed board design**, **drop and ingress reliability**, **thermal validation** and **build-to-build failure tracking**, with a test plan traced to every hardware requirement.
- Partners with **mechanical, firmware, scan engine and sourcing** teams, and travels to the **contract manufacturer** for every DVT and PVT build.
- Leads the **hardware design review** for the handheld team, mentors **2 junior engineers**, and wrote the **DVT reliability test spec** now used on 3 product lines.

## TECHNICAL SKILLS

| | |
|---|---|
| **EDA & Design Tools:** | Cadence Allegro, OrCAD, Altium Designer, Altium 365 |
| **Processors & Interfaces:** | Arm Cortex-A SoCs, LPDDR5, USB 3, MIPI CSI-2, MIPI DSI, PCIe, I2C |
| **Signal Integrity & Simulation:** | HyperLynx, Cadence Sigrity, LTspice, Ansys Icepak |
| **Lab & Debug Tools:** | Keysight oscilloscopes, USB and MIPI protocol analyzers, Lauterbach TRACE32, Python, thermal cameras |
| **Reliability & Validation Methods:** | HALT, FMEA, tumble and drop testing, IP68 testing, thermal shock, ESD testing |
| **Production & DFM:** | EVT/DVT/PVT, DFM, DFT, ICT, boundary scan, IPC-A-610 |
| **PLM, Sourcing & Compliance:** | Arena PLM, Jira, SiliconExpert, FCC Part 15, CE marking, UL 62368-1 |

## EDUCATION

**Stony Brook University** — **M.S. in Electrical Engineering** — Stony Brook, NY · Aug 2017 to May 2019

## WORK EXPERIENCE

### Zebra Technologies — Senior Hardware Engineer — Holtsville, NY · Mar 2022 to Present

- Set the hardware architecture for a rugged Android handheld, a 3-board split around the SoC, the scan engine and the battery that fit a housing **15%** thinner than the last model.
- Owned the 12-layer HDI main board in **Cadence Allegro**, with LPDDR5 and MIPI CSI-2 routing checked in HyperLynx, and released it with **0** rework fixes at DVT.
- Ran DVT from -20°C to 50°C on 40 units with **Python** stations logging battery, radio and scanner tests, and found **17** issues before the PVT build.
- Planned the IP68 and 1.8 m drop tests with the reliability lab, then moved a connector out of the corner impact zone and raised tumble test survival from 71% to **96%**.
- Led 3 builds at the contract manufacturer, EVT through PVT, and worked down the failure Pareto to cut line fallout from 7.5% to **2.1%** before mass production.

### Motorola Solutions — Hardware Engineer — Plantation, FL · Jul 2019 to Feb 2022

- Brought up the main board of a two-way radio over 4 prototype builds with the firmware team and a Lauterbach TRACE32 debugger, cutting boot failures per build from 11 to **2**.
- Replaced **23** end-of-life parts on a radio accessory family with the sourcing team, choosing drop-in alternates from SiliconExpert data and writing the ECOs.
- Agreed the connector, shield can and heat sink positions on a vehicle radio with mechanical engineers early, which took **1** full board spin out of the schedule.