Beatrice Whittle Lead Hardware Engineer

Round Rock, TX · beatrice.whittle@gmail.com · +1 512-555-0177 · linkedin.com/in/beatricewhittle

PROFILE SUMMARY

- **Lead Hardware Engineer** with **11 years** in server and storage hardware, leading **6 engineers** on the motherboard of a **2U PowerEdge server** at Dell Technologies through every build gate.
- Works in **Cadence Allegro**, **Cadence Sigrity** and **Ansys Icepak** on **Intel Xeon** and **AMD EPYC** platforms with DDR5, PCIe Gen5 and BMC subsystems.
- Known for **platform architecture trade studies**, **thermal and reliability sign-off**, **ODM build management** and **BOM cost-downs** that hold over a 5-year product life.
- Works with **mechanical, thermal, BIOS, BMC firmware and supply chain** teams in Round Rock and with **ODM engineers in Taiwan** on every EVT, DVT and PVT build.
- Chairs the **platform design review**, hires for the team, and has mentored **3 engineers** to senior since 2021.

TECHNICAL SKILLS

EDA & Design Tools:	Cadence Allegro, OrCAD Capture, Allegro Constraint Manager, Altium Designer
Processors & Interfaces:	Intel Xeon, AMD EPYC, DDR5 RDIMM, PCIe Gen5, CXL 2.0, OCP NIC 3.0, ASPEED BMC
Signal Integrity & Simulation:	Cadence Sigrity, HyperLynx, Ansys Icepak, Ansys SIwave, MATLAB
Lab & Debug Tools:	Keysight oscilloscopes, PCIe protocol analyzers, JTAG debug, Python, thermal cameras
Reliability & Validation Methods:	HALT, HASS, FMEA, shock and vibration, thermal cycling, MTBF modeling
Production & DFM:	EVT/DVT/PVT, DFM, DFT, ICT, boundary scan, IPC-A-610, ODM build management
PLM, Sourcing & Compliance:	Agile PLM, Jira, Confluence, FCC Part 15, CE marking, UL 62368-1, RoHS

EDUCATION

The University of Texas at Austin — **M.S. in Electrical and Computer Engineering** — Austin, TX · Aug 2013 to May 2015

WORK EXPERIENCE

Dell Technologies — Lead Hardware Engineer — Round Rock, TX · Apr 2020 to Present

- Set the motherboard architecture for a 2-socket 2U PowerEdge server, picking cabled PCIe Gen5 risers over retimers after a trade study that saved **$41** a unit.
- Owned the DVT plan for 4 motherboard variants, from DDR5 margining and PCIe Gen5 link tests to power-on cycling, and signed off DVT **2 weeks** ahead of the program date.
- Ran EVT, DVT and PVT builds with ODM engineers in Taiwan and brought ICT fallout down from 6.2% to **1.4%** by launch, mostly through DFT test point fixes.
- Took **$58** a unit out of the motherboard BOM with the sourcing team by qualifying second-source VRM parts and moving from a 20-layer to an 18-layer stackup.
- Worked with thermal engineers on fan zones and heat sinks for 350 W CPUs, using **Ansys Icepak** models that matched chamber data within **3°C**.

Western Digital — Hardware Engineer — San Jose, CA · Jun 2015 to Mar 2020

- Designed the controller board for **3** generations of enterprise NVMe SSDs in Allegro, with PCIe Gen4 routing checked in Cadence Sigrity before each fab release.
- Brought up the first prototypes of each SSD generation with firmware engineers, and a power sequencing fix cut boot failures at power-on from 9% to **0.2%**.
- Ran HALT and 1,000 thermal cycles on SSD prototypes with the reliability lab, and a capacitor package change fixed a solder crack seen in **4 of 40** units.