Bram van Dijk Senior FPGA Engineer

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PROFILE SUMMARY

- **Senior FPGA Engineer** with **7 years** in **semiconductors**, now designing the **video and Ethernet IP** in Microchip's **PolarFire SoC** reference designs, after building camera evaluation FPGAs for onsemi's **automotive image sensors**.
- Works in **SystemVerilog** and VHDL, builds in **Microchip Libero SoC** with Synplify Pro, verifies with **UVM** in QuestaSim, writes **SmartHLS** C++ for image math, and runs nightly builds from Tcl in **Jenkins**.
- Knows **MIPI CSI-2** camera pipelines, **fixed-point image processing** and **transceiver bring-up**, signs off CDC with **SpyGlass**, and starts each block with a spec that lists its clocks, resets and resource budget.
- Works with the **Linux BSP team**, **board designers** and applications engineers, leads the weekly **RTL design review** for the video IP group, and handles customer support cases that need an RTL fix.
- Mentors **3 engineers** on UVM and timing reports, wrote the team's **IP release checklist** (lint, CDC, coverage, timing), and signs off each video IP release for the **Libero IP catalog**.

TECHNICAL SKILLS

HDLs & Scripting:	SystemVerilog, VHDL, Verilog, Tcl, Python, C++
FPGA Tools & Devices:	Microchip Libero SoC, PolarFire SoC, PolarFire, Quartus Prime, Intel Arria 10 and Cyclone V, AMD Vivado (basics)
Verification Tools:	UVM, QuestaSim, SystemVerilog assertions, functional coverage, cocotb
Timing & CDC Tools:	Static timing analysis, SDC constraints, Synplify Pro, SpyGlass CDC, Questa CDC, Libero floorplanning
Interfaces & Protocols:	AXI4, AXI4-Stream, MIPI CSI-2, 10GBASE-R Ethernet, DDR4, PCIe Gen2
DSP & HLS:	SmartHLS, MATLAB, fixed-point modeling, image scaling, color correction
Embedded, Lab & CI:	RISC-V (PolarFire SoC CPU cluster), Yocto, SmartDebug, Signal Tap, Git, Jenkins

EDUCATION

Delft University of Technology — **M.Sc. in Electrical Engineering (Microelectronics)** — Delft, Netherlands · Sep 2017 to Aug 2019

WORK EXPERIENCE

Microchip Technology — **Senior FPGA Design Engineer** — Chandler, AZ · Mar 2022 to Present

- Wrote the **SystemVerilog** video pipeline for the **PolarFire SoC** Video Kit reference design, from the **MIPI CSI-2** receiver to the scaler, as parameterized IP that **6** later reference designs reuse.
- Built a **UVM** testbench in **QuestaSim** for the video IP with random frame sizes, pixel formats and back-pressure, closing functional coverage at **97.3%** before each IP catalog release.
- Moved the image scaler from hand-written RTL to **SmartHLS** C++ checked against a **MATLAB** fixed-point model, so adding a scaling mode went from 3 weeks to **4 days**.
- Added an **AXI4** frame DMA into DDR4 for the **RISC-V** cores, with a register map agreed with the Linux driver team, cutting CPU load per 1080p60 stream from 38% to **7%**.
- Brought up **10GBASE-R** Ethernet on the PolarFire transceivers for a video-over-IP design, tuning equalization from **SmartDebug** eye scans until the link ran 72 hours with **0** CRC errors.

onsemi — **FPGA Engineer** — Phoenix, AZ · Sep 2019 to Feb 2022

- Retimed the HDR merge datapath and rewrote the **SDC** constraints for the Intel **Arria 10** FPGA on the automotive camera evaluation boards in **Quartus Prime**, raising Fmax from 164 to **223 MHz**.
- Added reset synchronizers between the sensor and system clock domains after a start-up hang, checked them in **Questa CDC**, and ran **3,000** power cycles on the lab rack with no repeat.
- Brought up each new sensor sample with **Signal Tap** and a scope, and wrote **Python** register tests so the lab's sensor checkout went from 3 days to **1 day**.