Magnus Östlund Lead FPGA Engineer

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PROFILE SUMMARY

- **Lead FPGA Engineer** with **15 years** in **defense electronics** at BAE Systems and MITRE, now leading FPGA design for an **airborne electronic warfare receiver**, and holds an **active Secret clearance**.
- Sets the team's flow for **VHDL-2008** RTL, **AMD Vivado** builds from Tcl in Jenkins, **UVM** and cocotb tests in QuestaSim and **JasperGold** formal, with a **MATLAB** model behind each DSP block.
- Expert in **wideband channelizers**, **RF data converter** sync, **DO-254 DAL B** design assurance and **SEU mitigation** (TMR, configuration scrubbing) for airborne hardware, and sizes every device against a DSP and timing budget.
- Works with **systems engineering**, the RF, board and embedded software teams and the **program office**, reports FPGA status at each **PDR and CDR**, and chairs the weekly **FPGA design review**.
- Leads **7 FPGA engineers** and hired **4** of them, wrote the team's **VHDL coding and CDC guidelines**, and has mentored 3 engineers into senior roles since 2021.

TECHNICAL SKILLS

HDLs & Scripting:	VHDL-2008, SystemVerilog, Verilog, Tcl, Python, C++
FPGA Tools & Devices:	AMD Vivado, Vitis, Zynq UltraScale+ RFSoC and MPSoC, Kintex UltraScale, Versal
Verification Tools:	UVM, QuestaSim, cocotb, JasperGold, SystemVerilog assertions, IBM DOORS Next
Timing & CDC Tools:	Static timing analysis, XDC constraints, Pblock floorplanning, SpyGlass CDC and RDC
Interfaces & Protocols:	AXI4, JESD204B/C, RF-ADC and RF-DAC, 100G Ethernet, PCIe Gen3, Aurora 64B/66B, VITA 49
DSP & HLS:	MATLAB, Simulink, HDL Coder, Vitis HLS, polyphase channelizers, FFTs, pulse detection
Embedded, Lab & CI:	PetaLinux, Vivado ILA, Soft Error Mitigation IP, MicroBlaze, Git, Jenkins, spectrum analyzers

EDUCATION

KTH Royal Institute of Technology — M.Sc. in System-on-Chip Design — Stockholm, Sweden · Aug 2009 to Jun 2011

University of New Hampshire — B.S. in Electrical Engineering — Durham, NH · Sep 2005 to May 2009

WORK EXPERIENCE

BAE Systems — Lead FPGA Engineer — Nashua, NH · Apr 2018 to Present

- Set the FPGA architecture of an EW digital receiver on **Zynq UltraScale+ RFSoC**, folding 3 Kintex-7 FPGAs and 2 ADC cards into 1 device and cutting receiver power by **38%**.
- Led the bring-up of all 8 **RF-ADC** channels with multi-tile sync and a matched LMK04828 clock tree, holding channel-to-channel phase error under **1.6 degrees** after every power cycle.
- Set up requirements-based verification for the **DO-254 DAL B** receiver FPGA, tracing every **UVM** test to a requirement in **DOORS Next**, and cut design assurance audit findings from 27 to **4**.
- Floorplanned the channelizer with **Pblocks** and moved the team to scripted **Tcl** builds in Jenkins, raising the share of nightly **Vivado** runs that meet timing at 491.52 MHz from 58% to **96%**.
- Made **SpyGlass CDC** and reset checks a release gate across the receiver's 14 clock domains, and the lab has logged **0** clock-crossing bugs in the 26 months since.

MITRE — Senior FPGA Engineer — Bedford, MA · Aug 2011 to Mar 2018

- Hand-mapped a 64-channel polyphase channelizer from its **MATLAB** model onto DSP48E2 slices on **Zynq UltraScale+** for a sponsor's spectrum monitoring prototype, using **27%** fewer slices than the HDL Coder version.
- Brought up **PetaLinux** on the Zynq UltraScale+ ARM cores with an AXI DMA path from the channelizer, so sponsor analysts could record all 64 channels to NVMe at **1.4 GB/s**.
- Traced **JESD204B** link drops between an AD9625 ADC and a Kintex UltraScale FPGA to SYSREF timing with **Vivado ILA** and a scope, after the lab had been stuck on them for **5 weeks**.