Salma Bouchareb Junior FPGA Engineer

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PROFILE SUMMARY

- **Junior FPGA Engineer** with **3 years** at **Achronix**, designing and testing the **PCIe and GDDR6 reference designs** shipped with the **Speedster7t** tools, after a summer internship in **FPGA prototyping** at MaxLinear.
- Writes **SystemVerilog** and reads **VHDL**, builds in **Achronix ACE** with Synplify Pro, tests in **QuestaSim** and **cocotb**, and scripts builds and lab runs in **Tcl and Python** with Git and Jenkins.
- Knows the Speedster7t **2D network on chip** and the **MLP blocks** for int8 math, writes a short **design spec** before starting RTL, and keeps every block **lint and CDC clean** before review.
- Works with **applications engineers** and the **ACE software team**, settles each **register map** with the driver developers before writing logic, and presents new blocks at the weekly **RTL review**.
- Coached **1 summer intern** through the cocotb setup in 2025, wrote the team's **Snapshot debug guide**, and is learning the **UVM** flow the verification group uses on larger IP.

TECHNICAL SKILLS

HDLs & Scripting:	SystemVerilog, VHDL (reading and small fixes), Tcl, Python, C
FPGA Tools & Devices:	Achronix ACE, Speedster7t AC7t1500, Quartus Prime (internship), AMD Vivado (school projects)
Verification Tools:	cocotb, QuestaSim, SystemVerilog assertions, Verilator, UVM (learning)
Timing & CDC Tools:	Static timing analysis, SDC constraints, Synplify Pro, Questa CDC
Interfaces & Protocols:	AXI4, AXI4-Stream, PCIe, GDDR6, SPI, I2C
DSP & HLS:	MATLAB, fixed-point modeling, Speedster7t MLP blocks, FIR and decimation filters
Embedded, Lab & CI:	Achronix Snapshot, Signal Tap, oscilloscopes, Git, Jenkins

EDUCATION

San José State University — **B.S. in Computer Engineering** — San Jose, CA · Aug 2019 to May 2023

WORK EXPERIENCE

Achronix Semiconductor — **FPGA Design Engineer** — Santa Clara, CA · Jul 2023 to Present

- Wrote the **SystemVerilog** for a scatter-gather **AXI4** DMA engine in the Speedster7t **PCIe** reference design, moving host data into GDDR6 memory at **21.7 GB/s**.
- Built **cocotb** tests in **QuestaSim** for the descriptor logic, with random descriptor chains, error injection and an AXI4 memory model, raising functional coverage from 71% to **94%**.
- Added 2 pipeline stages to the descriptor fetch path and fixed false-path **SDC** constraints in **ACE**, taking worst negative slack at 500 MHz from -412 ps to **+38 ps**.
- Ran **Questa CDC** on the DMA block before each release and swapped 2 unsafe crossings between the NoC and user clocks for **async FIFOs**, clearing all **17** reported violations.
- Brought the design up on the **VectorPath** card with the **Snapshot** debugger and wrote **Python** lab scripts that cut the board test for each ACE release from 2 days to **7 hours**.

MaxLinear — **FPGA Engineering Intern** — Carlsbad, CA · Jun 2022 to Aug 2022

- Turned a **MATLAB** fixed-point model of a decimation filter into **VHDL** on a Cyclone V board in **Quartus Prime**, matching the model output on all **4,096** test vectors.
- Wrote **Tcl** and **Python** scripts that ran the prototyping team's nightly Quartus builds and posted timing summaries to the team channel, saving about **40 minutes** of checks each morning.
- Found a clock polarity mismatch on the SPI bus between the FPGA test board and an RF transceiver with **Signal Tap** and a scope, which unblocked **3** lab test plans.