Hyun-Woo Kim Senior Electrical Engineer

Ann Arbor, MI · hyunwoo.kim@gmail.com · +1 734-555-0189 · linkedin.com/in/hyunwookim

PROFILE SUMMARY

- **Senior Electrical Engineer** with **7 years** in **EV power electronics**, now designing **onboard charger** hardware at Rivian after almost 3 years on **48 V and 12 V** power boards at General Motors.
- Designs in **Altium Designer**, models in **Simulink**, **PLECS** and **LTspice**, checks parasitics in **Ansys Q3D**, and automates bench and HIL tests in **LabVIEW** and **Python**.
- Strong in **SiC power stages**, **totem-pole PFC**, isolated gate drives and **EMI filter** design, with parts picked to **AEC-Q100** and AEC-Q101 grades and a second source wherever one exists.
- Works with **controls firmware**, **thermal** and **vehicle integration** teams through **B-sample and C-sample** builds, and owns the charger's interface spec with the battery team.
- Mentors **2 engineers** on gate drive layout, co-leads the **power electronics design review**, and wrote the team's **SiC double-pulse test guide**.

TECHNICAL SKILLS

Schematic & PCB Tools:	Altium Designer, Altium 365, Xpedition (GM programs)
Simulation & Analysis:	Simulink, PLECS, LTspice, Ansys Q3D, MATLAB
Power Conversion:	Totem-pole PFC, CLLC and LLC converters, SiC MOSFETs, isolated gate drivers, 48 V DC-DC, EMI filters
Analog & Signal Chain:	Shunt and Hall current sensing, isolated amplifiers, 16-bit ADCs, active filters
Interfaces & Microcontrollers:	CAN FD, SPI, TI C2000, Infineon AURIX (hardware side)
Lab & Test Equipment:	Yokogawa WT5000, double-pulse test rig, LabVIEW HIL benches, thermal chambers, Python
Compliance Standards:	CISPR 25, ISO 7637-2, ISO 16750, AEC-Q100, AEC-Q101, ISO 26262 hardware metrics

EDUCATION

University of Michigan — **M.S. in Electrical and Computer Engineering** — Ann Arbor, MI · Sep 2017 to May 2019

WORK EXPERIENCE

Rivian — **Senior Electrical Engineer, Power Electronics** — Plymouth, MI · Mar 2022 to Present

- Led the power stage design of the onboard charger's **totem-pole PFC** and **CLLC** stages on SiC MOSFETs, raising peak efficiency from 94.8% to **96.6%** at full load.
- Designed the gate driver and isolated sensing board in **Altium Designer**, choosing AEC-Q100 parts with a second source for every IC, which cut the board's BOM cost by **$6.80** a unit.
- Built **Simulink** and **PLECS** models of the PFC current loop and matched them to bench data within **3%**, so controls could try loop changes in simulation before touching a board.
- Cut the charger's conducted emissions with a two-stage EMI filter and a new common-mode choke, clearing **CISPR 25** Class 5 limits with **6 dB** of margin on the first chamber visit.
- Brought up B-sample chargers on a **LabVIEW** HIL bench with a **Yokogawa WT5000**, running thermal and line-sag profiles that found **9** faults before vehicle testing began.

General Motors — **Electrical Engineer** — Warren, MI · Jul 2019 to Feb 2022

- Reviewed the layout of a **48 V** mild hybrid DC-DC board with the PCB team, moving the power loop onto inner layers and cutting switch-node overshoot from 22 V to **9 V**.
- Designed current sensing for a 12 V battery monitor with a **shunt** and a **16-bit** ADC, holding measurement error under **0.5%** from -40°C to 105°C.
- Ran DFM reviews with the Tier 1 supplier on **2** vehicle programs and closed 31 ECOs, raising end-of-line test yield from 95.2% to **98.7%**.