Hyun-woo Park Senior ASIC Design Engineer

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PROFILE SUMMARY

- **Senior ASIC Design Engineer** with **7 years** in **SoC and networking silicon**, now owning **display pipeline RTL** for Apple's **iPhone and Mac chips**, after building packet engines for **AWS Nitro** cards at Annapurna Labs.
- Writes **SystemVerilog**, synthesizes in **Fusion Compiler**, signs off timing in **PrimeTime**, writes **UPF** and checks CDC in **SpyGlass**, with **JasperGold** for control logic that random tests can't reach.
- Knows **pixel pipelines**, **multi-clock design** and **low-power design** on TSMC N3E, and writes each block's microarchitecture spec with its area, power and latency budget before the RTL.
- Works with **display architects**, **DV**, **physical design** and the **display driver team**, and runs the biweekly RTL review for the display pipeline across 2 SoC programs.
- Mentors **3 engineers** on timing closure and UPF, wrote the display team's **UPF handbook**, and reviews every new block spec before anyone starts writing RTL.

TECHNICAL SKILLS

Languages & Scripting:	SystemVerilog, Verilog, Python, Tcl, Perl
Simulation & Formal:	UVM, Synopsys VCS, Synopsys Verdi, JasperGold, SystemVerilog Assertions
Synthesis & STA:	Fusion Compiler, Design Compiler, PrimeTime, SDC constraints, MCMM sign-off
Lint, CDC & Power Intent:	SpyGlass CDC, SpyGlass RDC, SpyGlass Lint, UPF (IEEE 1801), VC LP
DFT & Test:	Scan insertion, MBIST, ATPG, Synopsys TestMAX
Buses & Interface IP:	AMBA AXI4, AXI4-Stream, APB, PCIe Gen4, MIPI DSI
Process & Physical Design:	TSMC N3E, TSMC N7, floorplan reviews, Synopsys IC Compiler II reports

EDUCATION

KAIST (Korea Advanced Institute of Science and Technology) — **M.S. in Electrical Engineering (VLSI Design)**

Daejeon, South Korea · Mar 2017 to Aug 2019

WORK EXPERIENCE

Apple — **Senior ASIC Design Engineer** — Sunnyvale, CA · Mar 2022 to Present

- Redesigned the display pipeline's **blend and dither** stages in **SystemVerilog** for **TSMC N3E** chips, sharing one multiplier array across 4 layers and cutting block area by **14%**.
- Closed the display pipeline at **1.1 GHz** with **Fusion Compiler** and **PrimeTime** sign-off, fixing a **-96 ps** worst path by splitting the gamma lookup across 2 cycles.
- Wrote the **UPF** for the display block's **4** power domains, with retention for frame state and clock gating on idle layers, cutting display power during video playback by **23%**.
- Rebuilt the pixel clock to fabric clock crossings with **async FIFOs** after a frame underflow showed up in emulation, then signed off **SpyGlass CDC** and RDC with **0** open waivers.
- Wrote **SVA** properties and **JasperGold** proofs for the layer arbiter with the DV team, finding **6** corner-case bugs that constrained-random **UVM** tests had missed.

Annapurna Labs (AWS) — **ASIC Design Engineer** — Austin, TX · Oct 2019 to Feb 2022

- Integrated a licensed **PCIe Gen4** controller and the **AXI4** interconnect into a **Nitro** card ASIC on TSMC N7, writing integration tests that found **9** wiring bugs before the full-chip build.
- Fixed scan blockers in the packet engine with the DFT team and added **MBIST** to **36** SRAMs, raising **TestMAX** stuck-at coverage on the block to **98.9%**.
- Debugged the packet engine on A0 silicon with **JTAG** and on-chip trace buffers, root-causing **3** silicon bugs that were fixed with metal-only ECOs before production.