Jovana Marković Lead ASIC Design Engineer

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PROFILE SUMMARY

- **Lead ASIC Design Engineer** with **11 years** in **networking and 5G modem silicon**, leading **8 engineers** on the data subsystem of Qualcomm's **Snapdragon modems** through **3 tape-outs** on TSMC N4 and N3E.
- Hands-on in **SystemVerilog**, **UVM** and **JasperGold** for verification, **Design Compiler** and **PrimeTime** for timing, **UPF** for power, and **SpyGlass** for CDC and RDC sign-off.
- Known for **subsystem microarchitecture**, **power and timing budgets** split across teams, and **A0 bring-up**, and puts every block through a written spec, a verification plan and a sign-off checklist.
- Works with **modem systems engineers**, **firmware**, **SoC integration** and **physical design**, and reports tape-out readiness to the program office at each milestone review.
- Hired **4** of the 8 engineers on the team, promoted **2** to senior, and chairs the modem group's **design review board** for new subsystem specs.

TECHNICAL SKILLS

Languages & Scripting:	SystemVerilog, Verilog, SystemC, Python, Tcl, Perl
Simulation & Formal:	UVM, JasperGold, Cadence Xcelium, Synopsys VCS, Synopsys Verdi
Synthesis & STA:	Design Compiler, Fusion Compiler, PrimeTime, Cadence Tempus, SDC constraints
Lint, CDC & Power Intent:	SpyGlass CDC, SpyGlass RDC, UPF (IEEE 1801), VC LP, Conformal LEC
DFT & Test:	Scan compression, ATPG, MBIST, Synopsys TestMAX, IEEE 1687
Buses & Interface IP:	AMBA AXI4, CHI, APB, network-on-chip, LPDDR5, PCIe Gen4
Process & Physical Design:	TSMC N4, TSMC N3E, TSMC 7nm and 16nm, Cadence Innovus budget and ECO reviews

EDUCATION

University of Belgrade, School of Electrical Engineering — **M.Sc. in Electronics and Microelectronics** — Belgrade, Serbia · Oct 2014 to Jul 2015

WORK EXPERIENCE

Qualcomm — Lead ASIC Design Engineer — San Diego, CA · Apr 2020 to Present

- Lead **8** ASIC engineers on the **5G modem** data subsystem for Snapdragon modems, owning its microarchitecture and RTL across **3** tape-outs on **TSMC N4** and N3E.
- Brought **JasperGold** formal sign-off to every arbiter and FIFO in the subsystem alongside **UVM** regressions, cutting bugs found late in emulation from 34 to **9** per tape-out.
- Drove the subsystem's **UPF** with the SoC power team, adding power gating for idle carrier paths and **DVFS** support, which cut its power in low-throughput modes by **27%**.
- Set block timing budgets with physical design so the subsystem closed **PrimeTime** sign-off at **1.6 GHz** on TSMC N4, **2 weeks** ahead of the tape-out date.
- Led A0 bring-up of the data subsystem in the San Diego lab with systems and firmware, triaging **22** silicon issues and getting every fix into the B0 stepping as a metal-only ECO.

Broadcom — ASIC Design Engineer — San Jose, CA · Sep 2015 to Mar 2020

- Integrated packet classification blocks with the **SerDes** and MAC IP on **Tomahawk** Ethernet switch ASICs at TSMC 16nm and 7nm, keeping full line rate on all **32** 400G ports.
- Owned **SpyGlass** CDC and RDC sign-off for the ingress pipeline across **14** clock domains, fixing crossings with async FIFOs and reset synchronizers until **0** unwaived violations were left.
- Worked with the DFT team on **scan compression** and **MBIST** for the packet buffers, reaching **99.1%** stuck-at coverage while keeping test time inside the tester budget.