Diya Krishnan Junior ASIC Design Engineer

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PROFILE SUMMARY

- **Junior ASIC Design Engineer** with **3 years** at **Tenstorrent**, writing and verifying the **AXI and APB peripherals** and small compute blocks that sit around the RISC-V cores on **AI accelerator chips**.
- Writes RTL in **SystemVerilog**, verifies it with **UVM** in **Cadence Xcelium**, runs block synthesis in **Cadence Genus**, and checks lint and CDC in **SpyGlass** before every RTL drop.
- Comfortable with **clock domain crossings**, **block-level timing fixes** and **coverage closure**, and starts each block with a one-page spec listing its ports, clocks, resets and registers.
- Works with **DV**, **physical design** and **firmware** engineers across the Austin and Toronto teams, joins the weekly RTL review, and helped on first-silicon bring-up in the lab.
- Runs **lint triage** for the peripheral team each release, wrote the **peripheral hub user guide** firmware codes against, and showed a summer intern how to set up the SpyGlass flow.

TECHNICAL SKILLS

Languages & Scripting:	SystemVerilog, Verilog, Python, Tcl, C (test code)
Simulation & Formal:	UVM, Cadence Xcelium, SystemVerilog Assertions, Verilator, Synopsys VCS (coursework)
Synthesis & STA:	Cadence Genus, Cadence Tempus, SDC constraints, Design Compiler (coursework)
Lint, CDC & Power Intent:	SpyGlass Lint, SpyGlass CDC, clock gating, UPF (reading and small edits)
DFT & Test:	Scan rules for RTL, Synopsys TestMAX (internship), JTAG
Buses & Interface IP:	AMBA AXI4, AXI4-Lite, APB, I2C, SPI, UART
Process & Physical Design:	TSMC N6, Cadence Innovus timing reports, Git, Jenkins

EDUCATION

The University of Texas at Austin — **B.S. in Electrical and Computer Engineering** — Austin, TX · Aug 2019 to May 2023

WORK EXPERIENCE

Tenstorrent — **ASIC Design Engineer** — Austin, TX · Jul 2023 to Present

- Wrote the **SystemVerilog** RTL for an **AXI4-Lite** peripheral hub (I2C, SPI, GPIO and timers) in the chip's management block, which **2** later chips reused with only parameter changes.
- Built the **UVM** agents and scoreboard for the peripheral hub in **Cadence Xcelium**, writing random register and bus traffic that took code coverage on the block to **98.4%**.
- Fixed **23** clock crossing violations on the always-on timer path with 2-flop synchronizers and a request and acknowledge handshake, then signed the block off in **SpyGlass CDC** with no waivers.
- Ran block synthesis in **Cadence Genus** and timing in **Tempus**, then moved logic out of **11** long paths in the APB bridge so the block met its 800 MHz target.
- Helped bring up the peripherals on first silicon in the Austin lab, writing **Python** tests over **JTAG** that cut the peripheral check from 2 days to **3 hours**.

SiFive — **ASIC Design Intern** — Santa Clara, CA · May 2022 to Aug 2022

- Added **clock gating** enables to **2** APB peripherals on a **RISC-V** core complex test chip, lowering their estimated dynamic power by **18%** in PrimePower.
- Integrated a **UART** and an **SPI** controller into the test chip's APB subsystem, writing the address map and **9** directed C tests that ran on the core in simulation.
- Ran scan insertion and **ATPG** on the intern block with the DFT team in **Synopsys TestMAX**, fixing 2 gated clocks that blocked scan and reaching **97.8%** stuck-at coverage.